Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**GATE**

**.025 X .018”**

**SOURCE**

**.032 X .024”**

**.115”**

**.082”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S= .032”X.024” G= .025”X.018”**

**Backside Potential: Drain**

**Mask Ref: HEX-2 100V GEN. 3**

**APPROVED BY: DK DIE SIZE .082” X .115” DATE: 7/11/22**

**MFG: INT’L RECTIFIER THICKNESS .015” P/N: IRFC120**

**DG 10.1.2**

#### Rev B, 7/19/02